IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3, 5, 8-11, 12-14, 16, 17, 22 and 23 and ADD new claims 25-28 in accordance with the following:

1. (CURRENTLY AMENDED) An information processing apparatus comprising:

a deciding unit that decides whether a given instruction ~~exists within a predetermined instruction set~~is one of a plurality of predetermined instructions;

a first operating unit that executes the instruction when the deciding unit decides that the instruction ~~exists within the predetermined instruction set;~~is one of the predetermined instructions;

a structure information output unit that outputs structure information for determining a circuit structure to execute the instruction when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set~~ is not one of the predetermined instructions; and

at least one second operating unit that ~~executes the instruction in~~ includes a plurality of combinational circuits and has the circuit structure determined based on the structure information output from the structure information output unit to execute the instruction, wherein

the structure information includes a plurality of parameters each of which determines an operation of each of the combinational circuits.

2. (ORIGINAL) The information processing apparatus according to claim 1, wherein the second operating units are provided in plurality.

3. (CURRENTLY AMENDED) The information processing apparatus according to claim 1, wherein when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set,~~ is not one of the predetermined instructions, the structure information output unit selectively outputs structure information for determining the circuit structure to execute the instruction, from among pieces of structure information.

4. (ORIGINAL) The information processing apparatus according to claim 3, wherein the structure information output unit selectively outputs structure information for determining the circuit structure to execute the instruction from among the structure information, based on any one of an address assigned by the instruction and an address held in a predetermined register of both.

5. (CURRENTLY AMENDED) The information processing apparatus according to claim 1, further comprising a rewritable memory ~~for storing~~that stores the structure information.

6. (ORIGINAL) The information processing apparatus according to claim 5, wherein in addition to the memory, the structure information is stored in a predetermined field within the instruction or in a predetermined register.

7. (ORIGINAL) The information processing apparatus according to claim 6, wherein each time when the second operating unit executes the instruction, a value held in the predetermined register is updated based on the structure information held in the memory.

8. (CURRENTLY AMENDED) The information processing apparatus according to claim 5, wherein the ~~instruction includes~~predetermined instructions include an instruction that instructs to load the structure information into the memory.

9. (CURRENTLY AMENDED) The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions; and

an instruction issuing unit that issues a plurality of instructions to load the structure information into the memory, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the instruction issuing unit.

10. (CURRENTLY AMENDED) The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions; and

an instruction issuing unit that issues an instruction to transfer the structure information to a predetermined register to which memory is allocated, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the instruction issuing unit.

11. (CURRENLTY AMENDED) The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions; and

an instruction issuing unit that issues an instruction to store the structure information in a predetermined area within an address space to which the memory is allocated, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory, wherein

the first operating unit executes the instruction issued by the instruction issuing unit.

12. (CURRENTLY AMENDED) The information processing apparatus according to claim 5, further comprising:

a second deciding unit that decides whether the instruction is an instruction to load the structure information into the memory when the deciding unit decides that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions; and

an instructing unit that instructs a DMA controller to transfer the structure information to the predetermined area within the address space to which the memory is allocated, when the second deciding unit decides that the instruction is the instruction to load the structure information into the memory.

13. (CURRENTLY AMENDED) The information processing apparatus according to

claim 1, wherein

the second operating unit ~~replaces optional bits within given data, in the circuit structure determined based on the structure information output from the structure information output unit~~includes a plurality of multiplexers to shuffle a plurality of bits in input data, and

the structure information includes a plurality of parameters that causes the multiplexers to output bits of mutually different positions in the input data.

14. (CURRENTLY AMENDED) The information processing apparatus according to claim 1, wherein

the structure information includes a first parameter and a second parameter, and

the second operating unit counts the number of 1s within ~~given~~ input data, and includes ~~in the circuit structure determined based on the structure information output from the structure information output unit~~

a right shifter that shifts the input data to the right by a predetermined number of bits determined by the first parameter;

a pattern generator that generates a predetermined mask pattern determined by the second parameter;

a first AND circuit that takes a first logical product of the input data and the predetermined mask pattern;

a second AND circuit that takes a second logical product of the input data, after being shifted by the right shifter, and the predetermined mask pattern; and

an adder that adds the first logical product and the second logical product.

15. (ORIGINAL) The information processing apparatus according to claim 1, further comprising a selecting unit that outputs only information at a predetermined bit position within the structure information output from the structure information output unit.

16. (CURRENTLY AMENDED) An information processing method comprising:

deciding whether a given instruction ~~exists within a predetermined instruction set~~is one of a plurality of predetermined instructions;

a first step of executing the instruction when it is decided at the deciding that the instruction ~~exists within the predetermined instruction set~~is one of the predetermined instructions;

~~outputing~~outputting structure information for determining a circuit structure to execute the

instruction when it is decided at the deciding that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions; and

a second step of executing the instruction ~~in~~ by an operating unit including a plurality of combinational circuits and having the circuit structure determined based on the structure information output at the outputting, wherein

the structure information includes a plurality of parameters each of which determines an operation of each of the combinational circuits.

17. (CURRENTLY AMENDED) The information processing method according to claim 16, wherein when it is decided at the deciding that the instruction ~~does not exist within the predetermined instruction set~~is not one of the predetermined instructions, then at the outputting, structure information is selectively output for determining the circuit structure to execute the instruction, from among pieces of structure information.

18. (ORIGINAL) The information processing method according to claim 17, wherein at the outputting, the structure information is selectively output based on at least one of an address assigned by the instruction and an address held in a predetermined register.

19. (ORIGINAL) The information processing method according to claim 16, wherein the structure information is held in a rewritable memory.

20. (ORIGINAL) The information processing method according to claim 19, wherein the structure information is held in a predetermined field within the instruction or in a predetermined register in addition to the memory.

21. (ORIGINAL) The information processing method according to claim 20, wherein each time when the instruction is executed at the second step, a value held in the predetermined register is updated based on the structure information held in the memory.

22. (CURRENTLY AMENDED) The information processing method according to claim 19, further comprising:

~~a third step of deciding that includes~~ deciding whether the instruction is an instruction to load the structure information into the memory when it is decided ~~at the deciding~~ that the instruction ~~does not exist within the predetermined instruction set~~ is not one of the

predetermined instructions; and

issuing a plurality of instructions to load the structure information into the memory when it is decided ~~at the third step~~ that the instruction is the instruction to load the structure information into the memory, wherein

~~at the first step,~~ the instruction issued at the issuing is executed.

23. (CURRENTLY AMENDED) The information processing method according to claim 19, further comprising:

~~a fourth step of~~ deciding whether the instruction is an instruction to load the structure information into the memory when it is decided at the deciding that the instruction ~~does not exist within the predetermined instruction set~~ is not one of the predetermined instructions; and

issuing an instruction to transfer the structure information to a predetermined register to which the memory is allocated when it is decided ~~at the fourth step~~ that the instruction is the instruction to load the structure information into the memory, wherein

~~at the first step,~~ the instruction issued at the issuing is executed.

24. (ORIGINAL) The information processing method according to claim 16, further comprising outputting of only information at a predetermined bit position within the structure information output at the outputting.

25. (NEW) The information processing apparatus according to claim 1, wherein the second operating unit performs a bit replacement operation according to the DES encryption algorithm and includes:

a right shifter that shifts a first input data to the right by a predetermined number of bits;

a pattern generator that generates a predetermined mask pattern;

an inverting circuit that inverts the predetermined mask pattern;

a first AND circuit that takes a first logical product of the first input data, after being shifted by the right shifter, and the predetermined mask pattern inverted by the inverting circuit;

a bit replacing unit that rearranges a plurality of bits in a second input data;

a second AND circuit that takes a second logical product of the input data, after rearranged by the bit replacing unit, and the predetermined mask pattern; and

an OR circuit that takes a logical sum of the first logical product and the second logical product.

26. (NEW) The information processing method according to claim 16, wherein

the operating unit includes a plurality of multiplexers to shuffle a plurality of bits in an input data, and

the structure information includes a plurality of parameters that causes the multiplexers to output bits of mutually different positions in the input data.

27. (NEW) The information processing method according to claim 16, wherein

the structure information includes a first parameter and a second parameter; and

the operating unit counts the number of 1s within an input data, and includes

a right shifter that shifts the input data to the right by a predetermined number of bits determined by the first parameter;

a pattern generator that generates a predetermined mask pattern determined by the second parameter;

a first AND circuit that takes a first logical product of the input data and the predetermined mask pattern;

a second AND circuit that takes a second logical product of the input data, after being shifted by the right shifter, and the predetermined mask pattern; and

an adder that adds the first logical product and the second logical product.

28. (NEW) The information processing method according to claim 16, wherein the operating unit performs a bit replacement operation according to the DES encryption algorithm, and includes

a right shifter that shifts a first input data to the right by a predetermined number of bits;

a pattern generator that generates a predetermined mask pattern;

an inverting circuit that inverts the predetermined mask pattern;

a first AND circuit that takes a first logical product of the first input data, after being shifted by the right shifter, and the predetermined mask pattern inverted by the inverting circuit;

a bit replacing unit that rearranges a plurality of bits in a second input data;

a second AND circuit that takes a second logical product of the input data, after rearranged by the bit replacing unit, and the predetermined mask pattern; and

an OR circuit that takes a logical sum of the first logical product and the second logical product.